TECHNICAL STAGE

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A New GaN/SiC Transistor Digitizer

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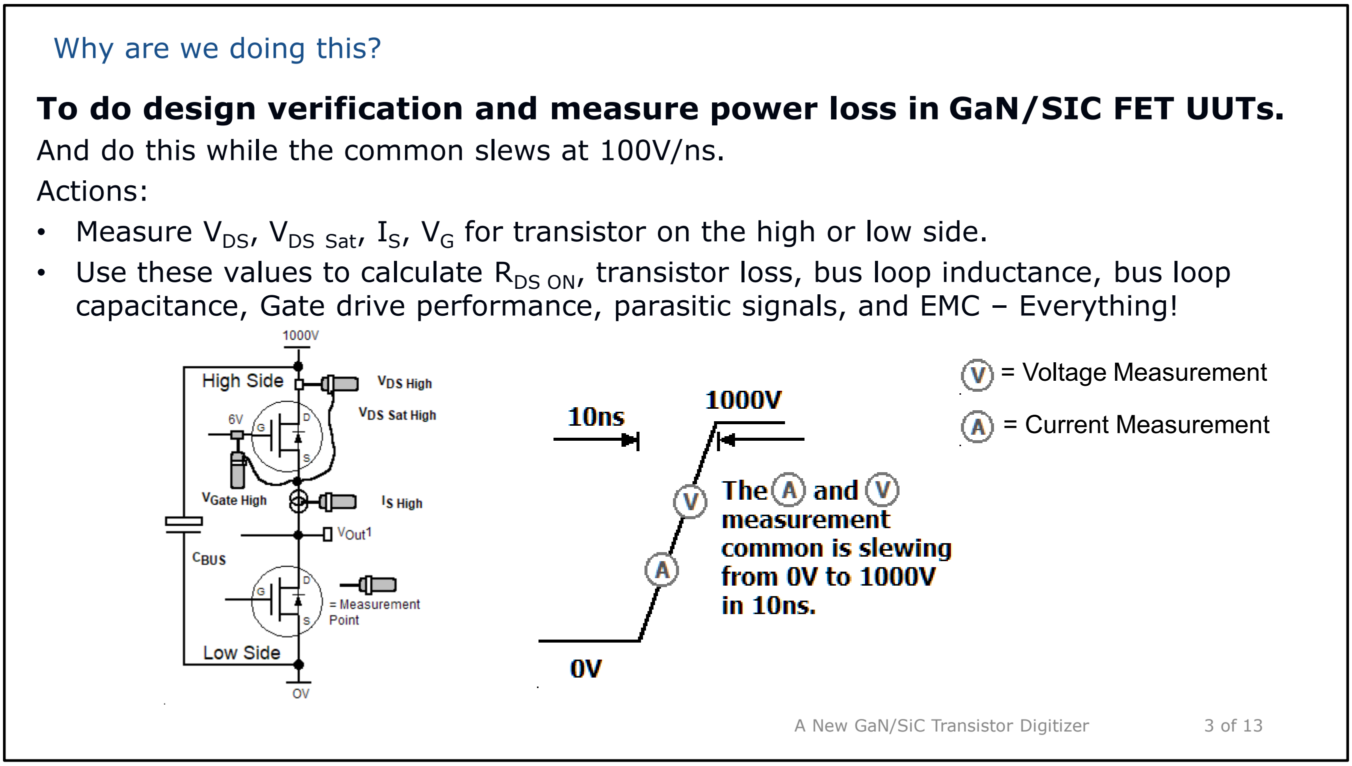

Why are we doing this?

To do design verification and measure power loss in GaN/SIC FET UUTs.

And do this while the common slews at 100V/ns.

Actions:

- Measure V_{DS}, $V_{DS\ Sat}$, I_S, V_G for transistor on the high or low side.
- Use these values to calculate $R_{DS\ ON}$, transistor loss, bus loop inductance, bus loop capacitance, Gate drive performance, parasitic signals, and EMC – Everything!

The A and V measurement common is slewing from 0V to 1000V in 10ns.

V = Voltage Measurement

A = Current Measurement

For the purposes of this presentation, we assume a 1000V voltage bus, with the UUT switching in 10ns. This is a slew rate of 100V/ns.

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Big Question 1 ?????

Say we are doing Double Pulse Testing.

The blue shading, on the edges, is where all the action is. Everything else happens rather slowly.

So, the big question 1:

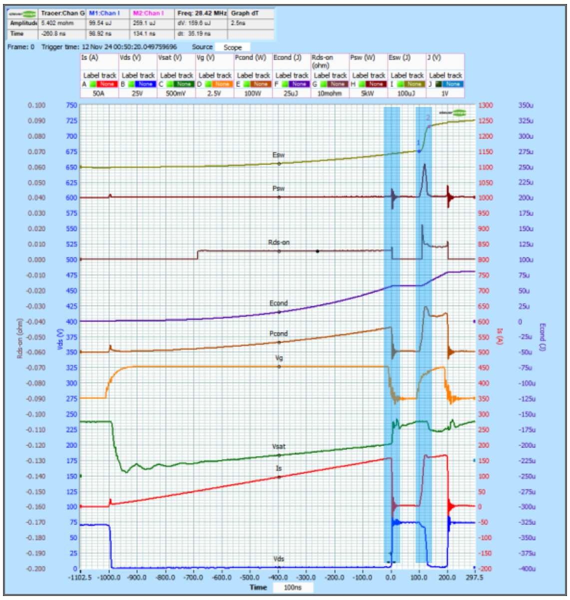
Why would you digitize all that slow stuff at high rate (say 5 GSPS)??

It just **costs** more FPGA, memory, transfer bandwidth and a good deal more money.

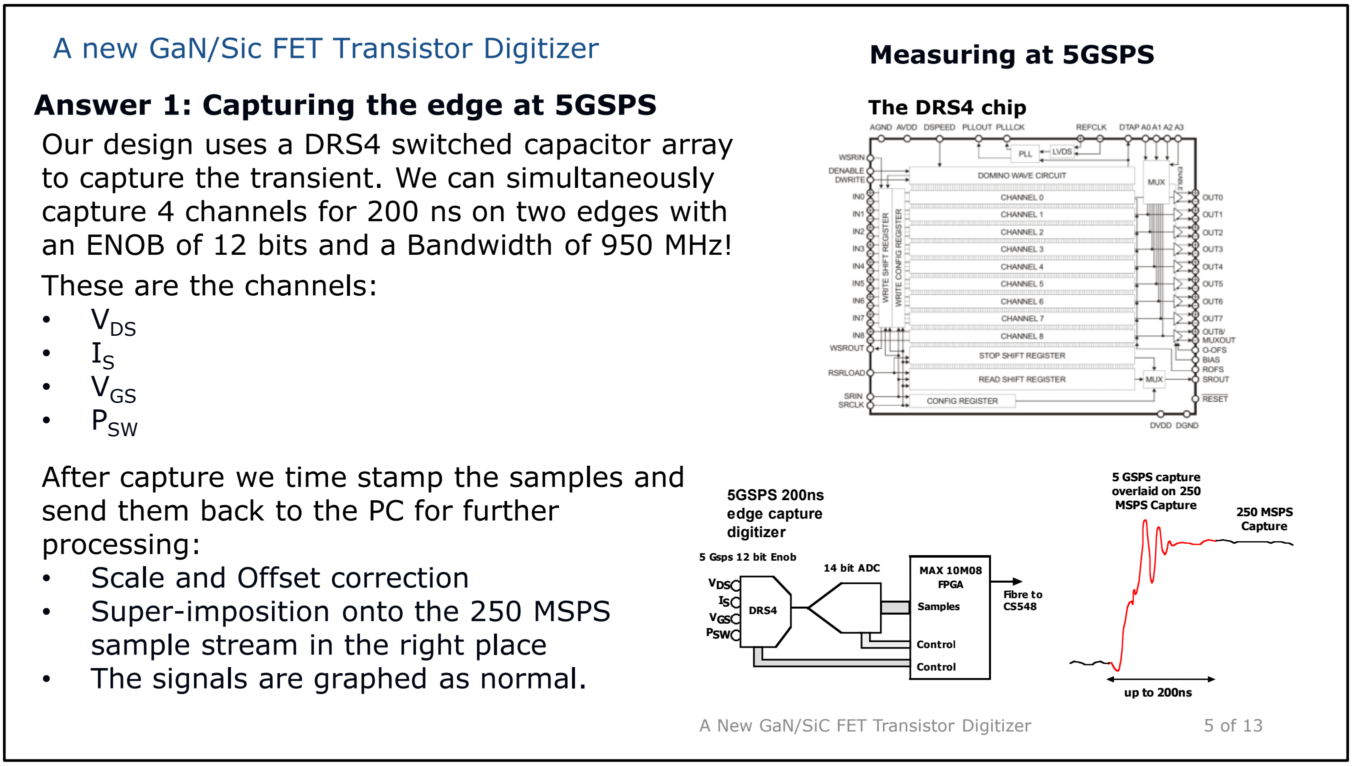
We wondered about this a lot! We have a solution:

- Digitize the blue shading at 5 GSPS
- Digitize the rest at 250 MSPS

Once and X 100k/sec



For the double pulse test, the two blue edges can be used to characterize the transistor, the bus loop inductance, and the gate drive at a given current. The current is easily changed by varying the initial pulse length, which sets the terminal current on the load inductor induced current ramp. We offer our Pulse builder which can easily generate up to 8 time coherent pulse patterns, which you draw on the screen, and then set the timing for.



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Answer 1: Capturing the edge at 5GSPS

Our design uses a DRS4 switched capacitor array to capture the transient. We can simultaneously capture 4 channels for 200 ns on two edges with an ENOB of 12 bits and a Bandwidth of 950 MHz!

These are the channels:

- V_{DS}
- I_S
- V_{GS}
- P_{SW}

After capture we time stamp the samples and send them back to the PC for further processing:

- Scale and Offset correction
- Super-imposition onto the 250 MSPS sample stream in the right place
- The signals are graphed as normal.

Measuring at 5GSPS

The DRS4 chip

5GSPS 200ns edge capture digitizer

5 GSPS capture overlaid on 250 MSPS Capture

250 MSPS Capture

up to 200ns

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The DRS4 is made by the Paul Scherrer institute in Switzerland. It has been primarily designed to capture short high energy physics events. It is used around the world. It is perfect for the transient capture we need to do here.

It has 9 channels, each of 1024 capacitive cells. These cells are sampled at 5 GSPS, or 200ps per cell. A 'domino' wave is used to connect each cell one at a time to the signal source. The capacitor voltages are then read out in slow time (31.25 MSPS in our case). We use a 14 bit ADC to do the readout, and maintain a 12 bit ENOB. The 9'th channel is used to capture a timing waveform that we use to synchronize the recorded waveform with the 250 MSPS captured waveform. We use 4 channels at a time – one for the second double pulse edge, and the second set of 4 channels for the 3rd double pulse edge. We can freeze the channel set not being used for capture. Each capture is 200ns in duration (1024 x 200ps). If the waveform being recorded is less than 400ns in length, we can link one channel to the next one to make a 400ns capture. In this way we will cover all the bases. Reconstruction is based on a very accurate timing system shared between the CS548 and all the channels.

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Big Question 2 ?????

DPT seems to be everything, but what about the real world? The UUT needs to be tested while it switches, for hours or days.

So, the big question 2:

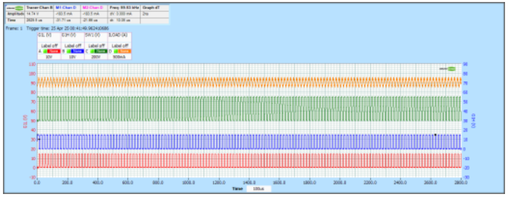
Why would you pay for an expensive DPT tester that does not do real world continuous testing?

DPT uses scopes that can’t record for days.

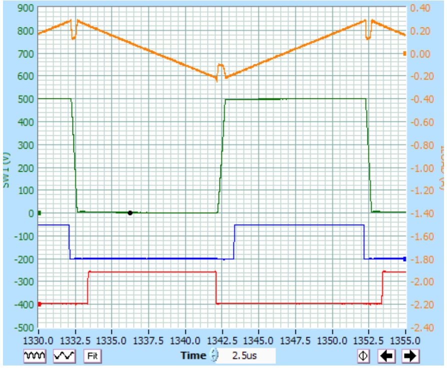
We wondered about this a lot! We have a solution:

- Include real time hardware that transfers the switch edge power and loss for every edge. For days!
- Use continuous 250 MSPS ADC’s and FPGA logic to derive pulse duration and conduction loss for every single pulse. For days!

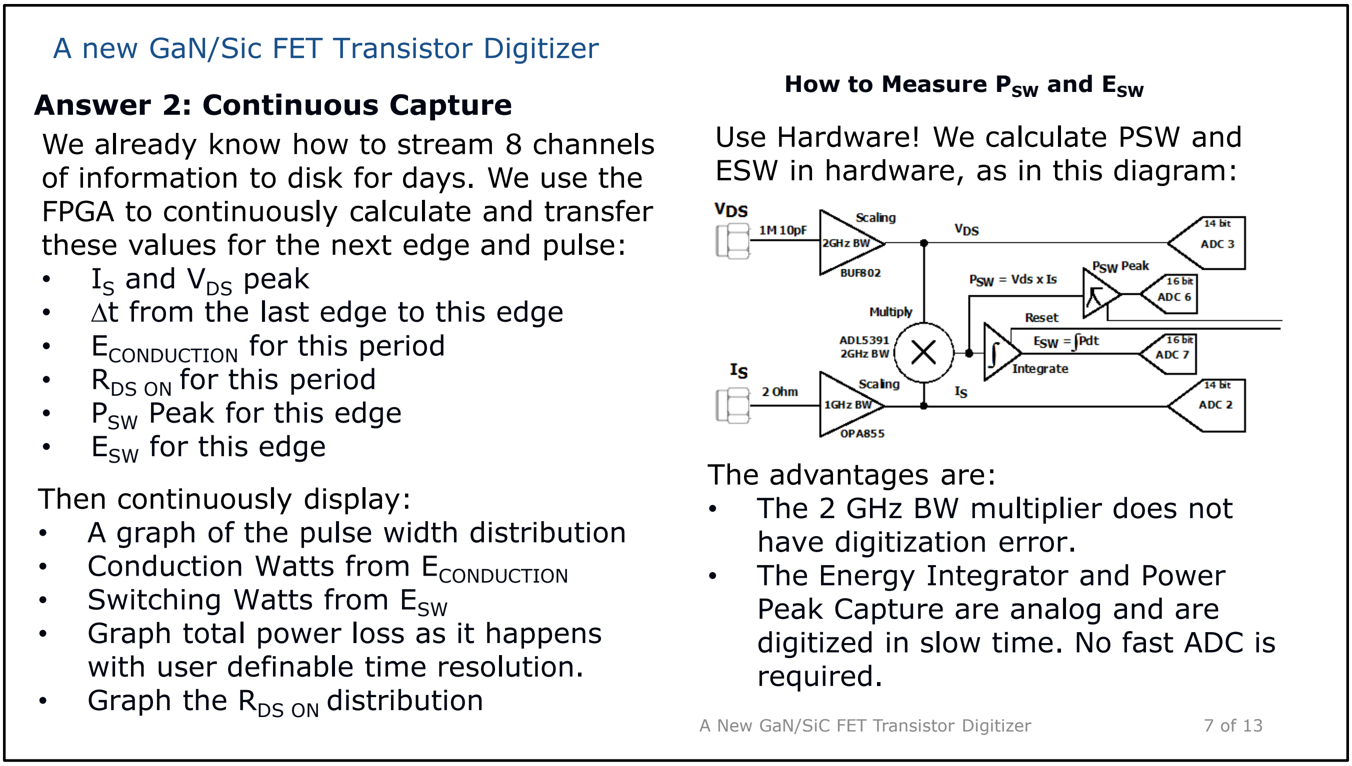
Days of this:



Being analysed at this time scale:



We started off just doing Double Pulse. But the real world has quite different use cases, and dynamic load conditions that do not occur in a double pulse test. We think measuring continuous operation will lead to greater reliability in the UUT – better understanding of the power dissipated, and the thermal constraints that come from that, and better understanding of the limits at which the transistor might operate in current and voltage.



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Answer 2: Continuous Capture

We already know how to stream 8 channels of information to disk for days. We use the FPGA to continuously calculate and transfer these values for the next edge and pulse:

- I_S and V_{DS} peak
- Δt from the last edge to this edge
- $E_{CONDUCTION}$ for this period
- $R_{DS\ ON}$ for this period
- P_{SW} Peak for this edge
- E_{SW} for this edge

Then continuously display:

- A graph of the pulse width distribution
- Conduction Watts from $E_{CONDUCTION}$
- Switching Watts from E_{SW}
- Graph total power loss as it happens with user definable time resolution.
- Graph the $R_{DS\ ON}$ distribution

How to Measure P_{SW} and E_{SW}

Use Hardware! We calculate PSW and ESW in hardware, as in this diagram:

The advantages are:

- The 2 GHz BW multiplier does not have digitization error.
- The Energy Integrator and Power Peak Capture are analog and are digitized in slow time. No fast ADC is required.

Using a hardware multiplier and hardware peak capture of the power and energy means we can measure GHz BW signals, while only needing slowish (2MSPS) ADC's to record the result. This means we get the real transient edge power. Very good time alignment is needed for this, so we control the length of each channel probe precisely. All the information we capture is available on every edge continuously. This would be very hard to do using a digitizing system such as a DSO.

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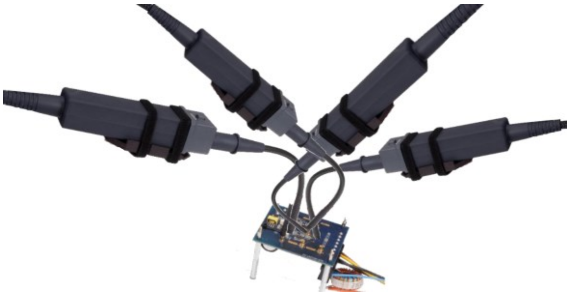
Big Question 3 ?????

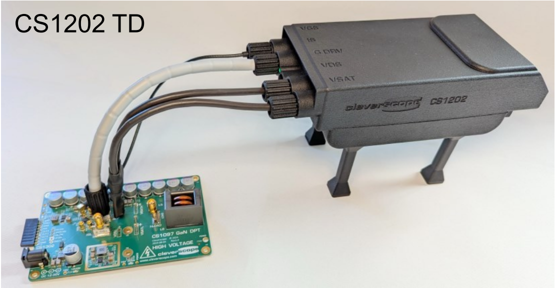


Say we are connected to the top transistor. Everything is referred to the Source.

So, the big question 3:

Why would you pay for 4 expensive probes to measure Vds, Vgs, Is, and Vsat?

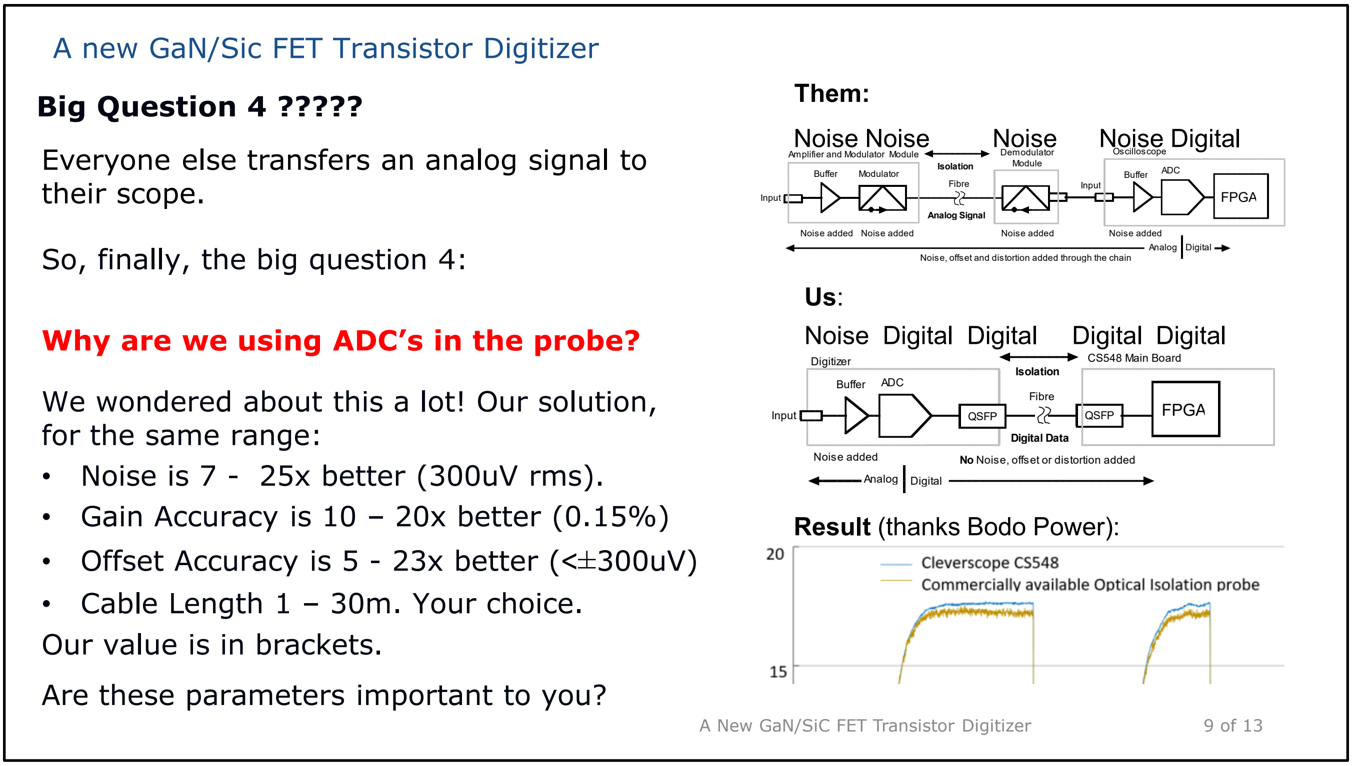
Oh wait ! There is **no** V_{SAT} probe. I_S probes use a huge coaxial shunt. Everything takes up a lot of room. The cost is increasing.



We wondered about this a lot! We have a solution:

- Put everything inside one box. Everything is referred to the source. **Much** less expensive.
- And so the CS1202 Transistor Digitizer is born!

Off course the CS1202 has to do all the functions – besides VDS and VGS, we have to measure current accurately with low insertion inductance. Knowing the DC helps for power measurement. To measure transistor conduction loss we need to know the On voltage accurately (we call it V_{SAT}).



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Big Question 4 ?????

Everyone else transfers an analog signal to their scope.

So, finally, the big question 4:

Why are we using ADC’s in the probe?

We wondered about this a lot! Our solution, for the same range:

- Noise is 7 - 25x better (300uV rms).
- Gain Accuracy is 10 – 20x better (0.15%)
- Offset Accuracy is 5 - 23x better (<±300uV)
- Cable Length 1 – 30m. Your choice.

Our value is in brackets.

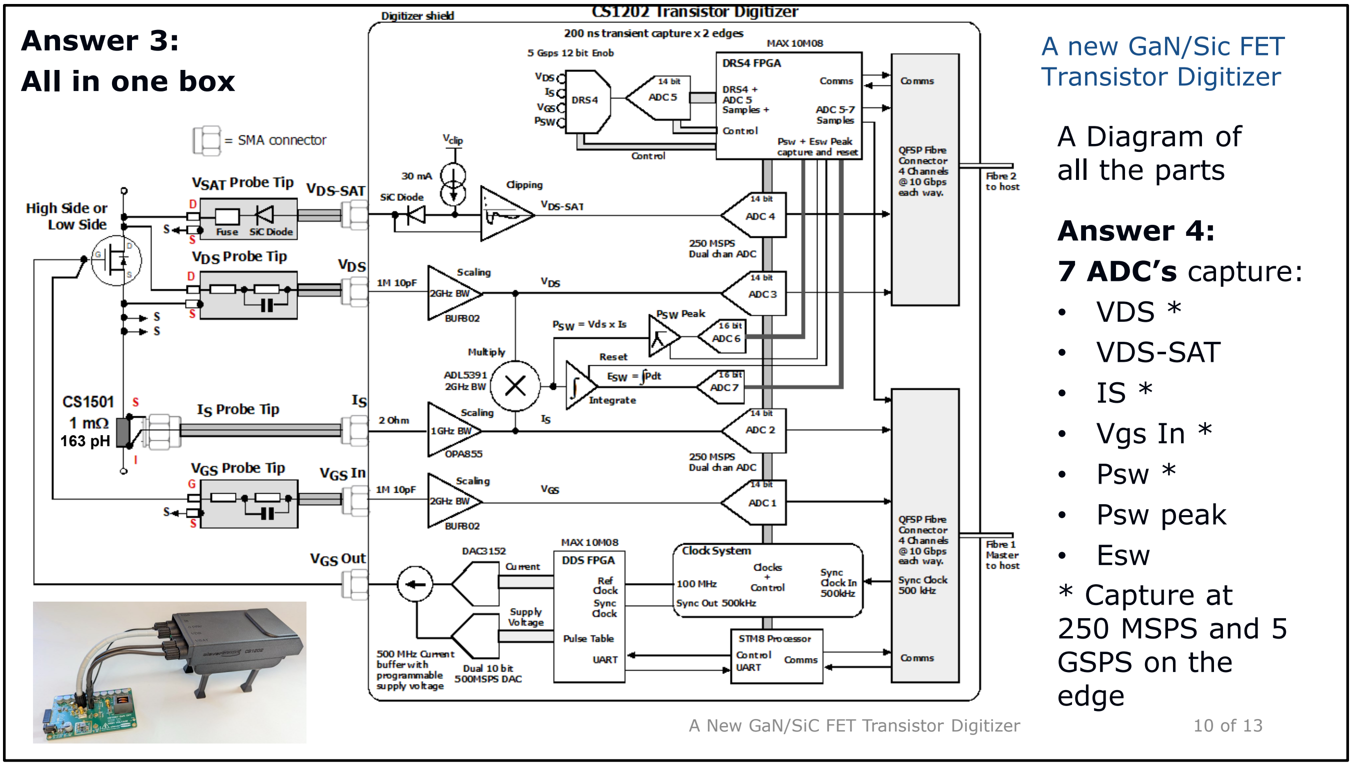
Are these parameters important to you?

Them:

Us:

Result (thanks Bodo Power):

Using an existing scope to measure an analog isolated signal does make sense. You already have the scope. But all the isolated fiber probes use a modulator followed by a demodulator, and then the noisy input to the scope. This all adds noise, offset, and gain error. But the accuracy of the scope multiplies the inaccuracy of calculations that use a division, such as $R_{DSON} = V_{ON}/I_S$. Von also needs to be known accurately for conduction power. Imagine a 1 mΩ FET conducting 1000A (it happens in cars). A mV makes a lot of difference. All of the parameters above become important.



Answer 3:
All in one box

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A Diagram of all the parts

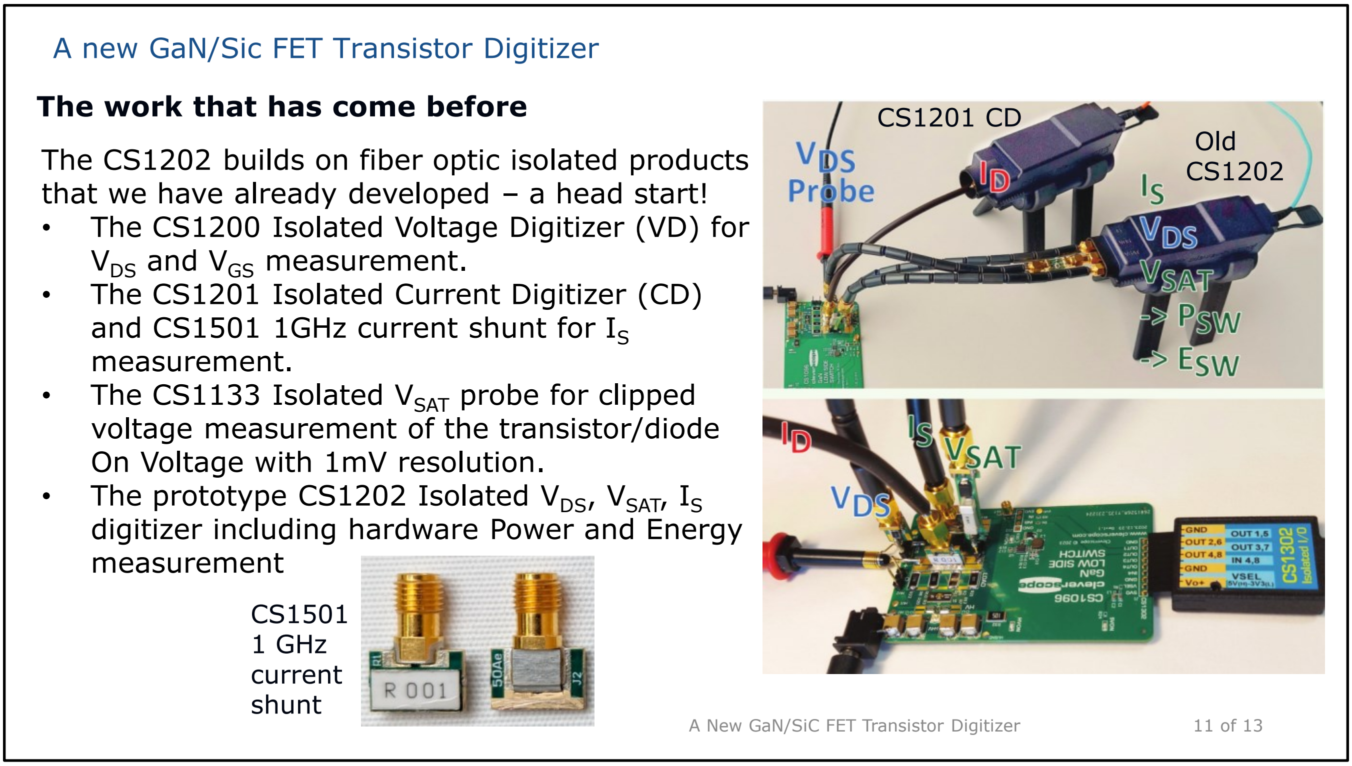
Answer 4:

7 ADC's capture:

- VDS *
- VDS-SAT
- IS *
- Vgs In *
- Psw *
- Psw peak
- Esw

* Capture at 250 MSPS and 5 GSPS on the edge

By putting all the ADC's in one box we can share timing between them, and share the FPGA resource between each function. We don't need separate packaging of each measurement function, saving a lot of space and cost. There is only one shared power system. Because the data is sent back via QSFP Active Optical Cables, we can manage cables varying in length from 1-30m.



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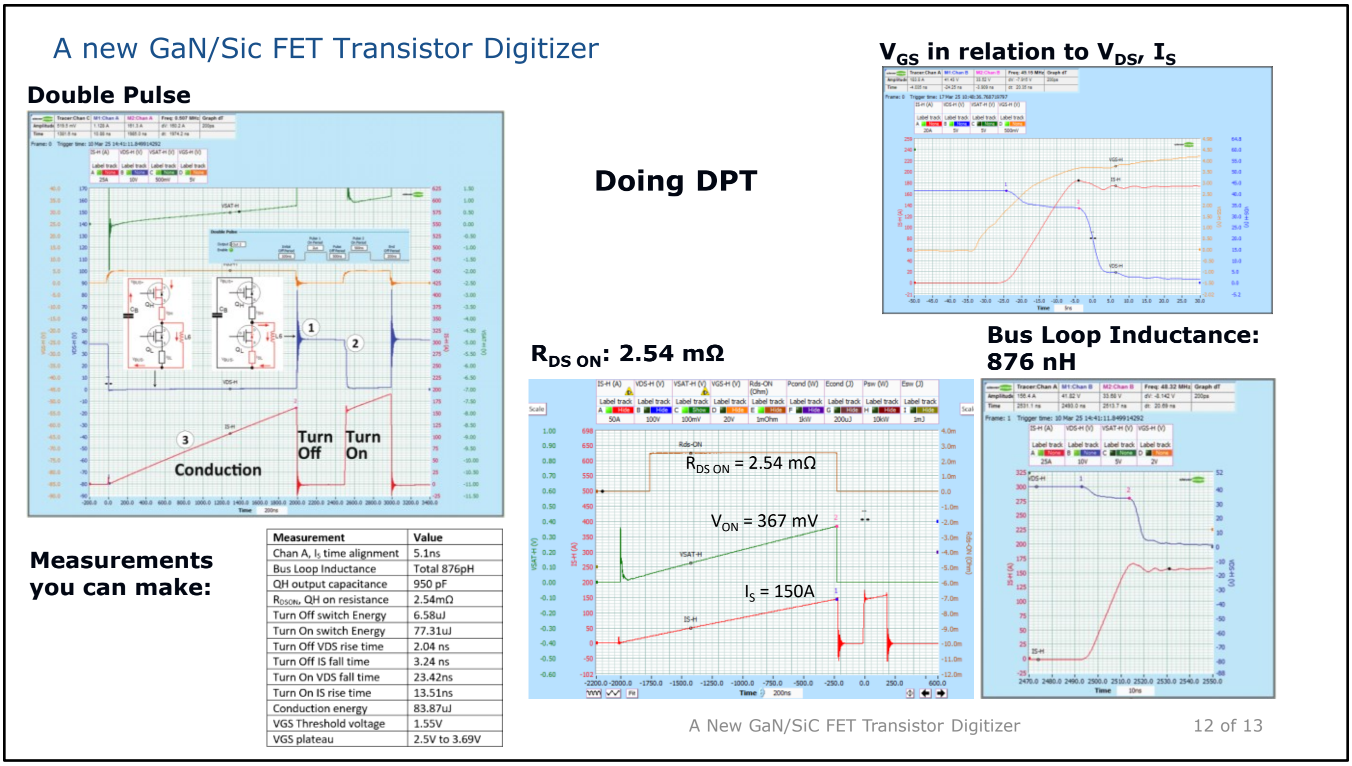
The work that has come before

The CS1202 builds on fiber optic isolated products that we have already developed – a head start!

- The CS1200 Isolated Voltage Digitizer (VD) for V_{DS} and V_{GS} measurement.
- The CS1201 Isolated Current Digitizer (CD) and CS1501 1GHz current shunt for I_S measurement.
- The CS1133 Isolated V_{SAT} probe for clipped voltage measurement of the transistor/diode On Voltage with 1mV resolution.
- The prototype CS1202 Isolated V_{DS}, V_{SAT}, I_S digitizer including hardware Power and Energy measurement

CS1501
1 GHz
current
shunt

Having been here before, and optimized each individual product function, we can be pretty sure that the CS1202 will work as expected.



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Double Pulse

Doing DPT

V_{GS} in relation to V_{DS}, I_S

$R_{DS\ ON}$: 2.54 mΩ

Bus Loop Inductance: 876 nH

Measurements you can make:

Measurement	Value
Chan A, I_S time alignment	5.1ns
Bus Loop Inductance	Total 876pH
QH output capacitance	950 pF
R_{DSON}, QH on resistance	2.54mΩ
Turn Off switch Energy	6.58uJ
Turn On switch Energy	77.31uJ
Turn Off VDS rise time	2.04 ns
Turn Off IS fall time	3.24 ns
Turn On VDS fall time	23.42ns
Turn On IS rise time	13.51ns
Conduction energy	83.87uJ
VGS Threshold voltage	1.55V
VGS plateau	2.5V to 3.69V

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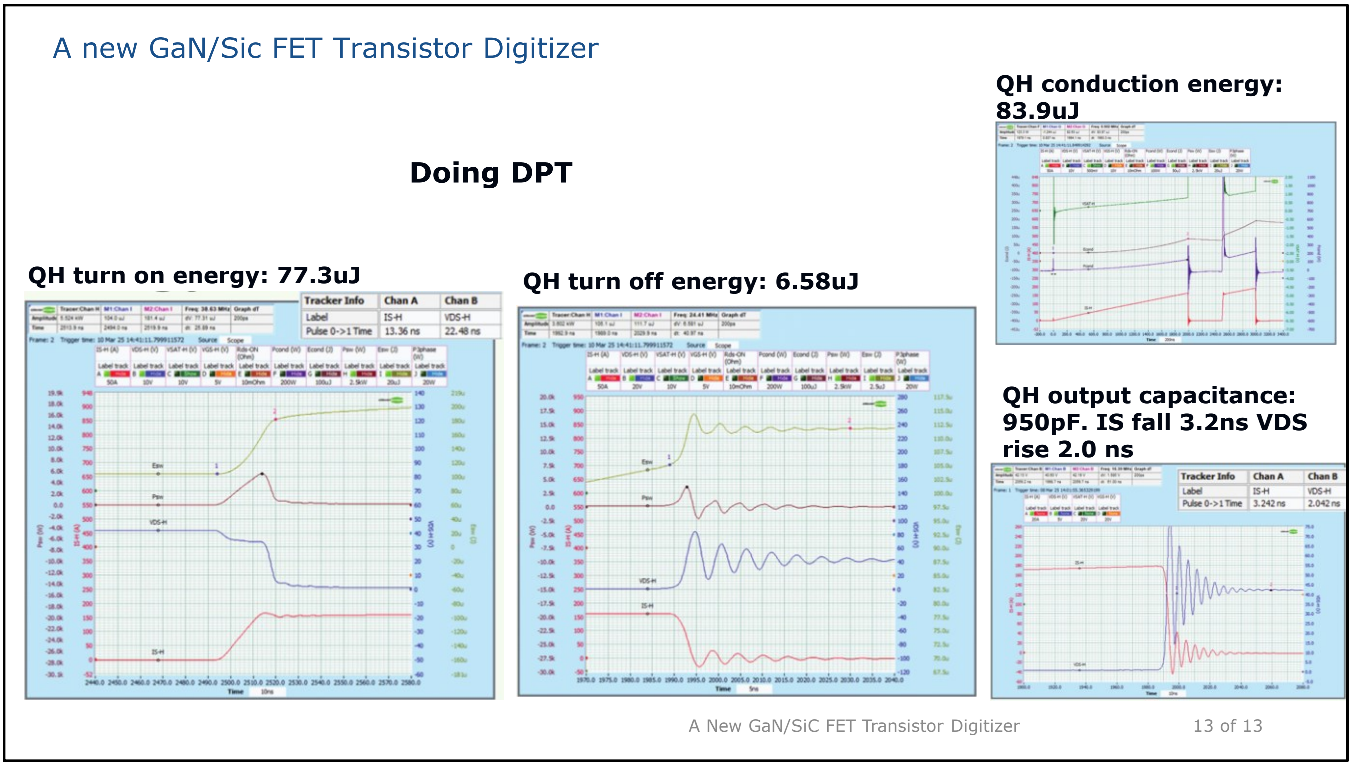
Using the equation $V = L\frac{di}{dt}$, we can re-arrange to $dt = L\frac{di}{V}$. With a fixed V (about 42V in this example), and L (470 nH) we find $dt = 470n\frac{di}{42}$. Say we want to get to 150A, dt = 1.7 us.
We use the Maths Equation builder to calculate $R_{DSON} = V_{ON}/I_S$. We can check the VGS threshold from graph = 1.55V. We can calculate the Bus loop inductance from $L_{bl} = (Vdc - Vds)\frac{dt}{di}$. For the numbers here L_{BL} = 876 nH. We can also observe the Miller plateau in the region where V_{DS} drops rapidly.
All of these functions will be automated soon.



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Doing DPT

QH turn on energy: 77.3uJ

Tracker Info	Chan A	Chan B
Label	IS-H	VDS-H
Pulse 0->1 Time	13.36 ns	22.48 ns

QH turn off energy: 6.58uJ

QH conduction energy: 83.9uJ

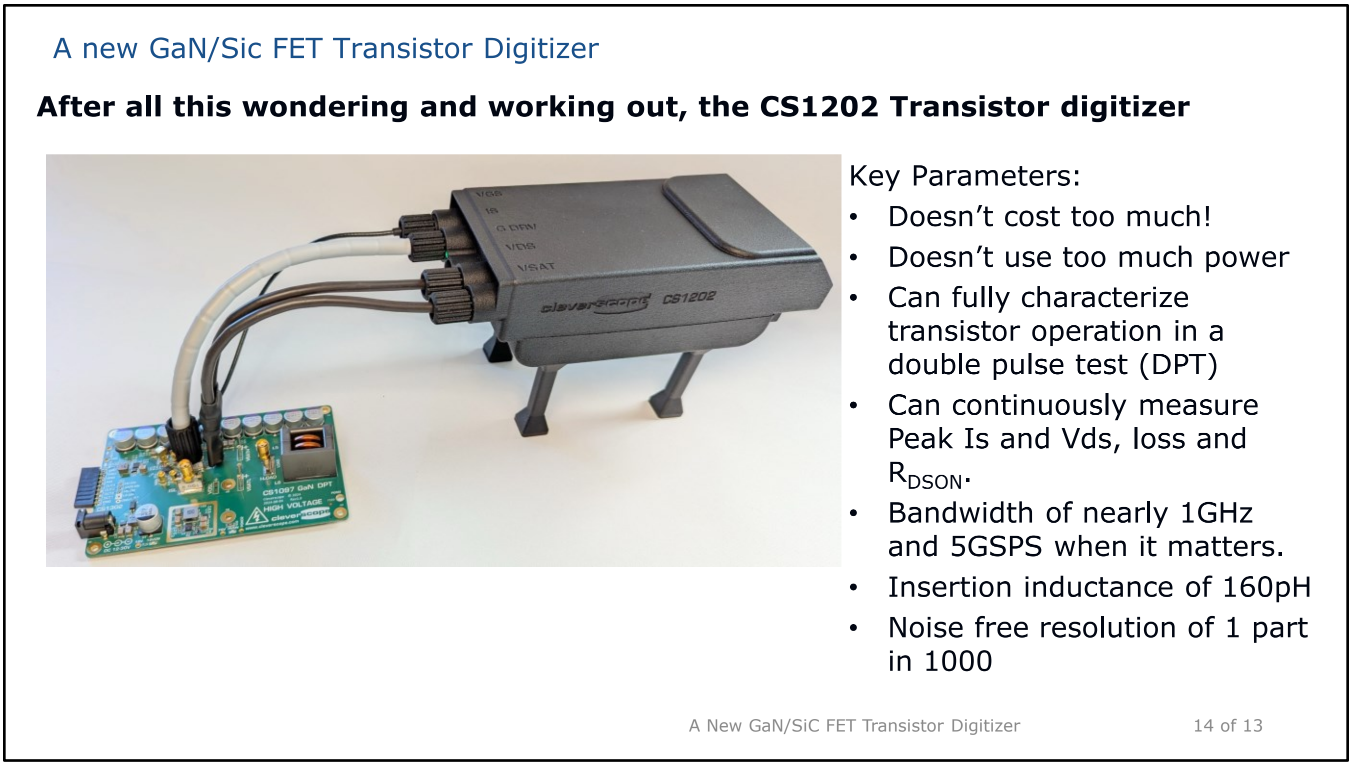
QH output capacitance: 950pF. IS fall 3.2ns VDS rise 2.0 ns

Tracker Info	Chan A	Chan B
Label	IS-H	VDS-H
Pulse 0->1 Time	3.242 ns	2.042 ns

We calculate the QH turn edge power as PSW = VDS x IS. The peak power has the tracer on it (5.52 kW). We integrate Power to get Energy, easy to do in Maths Equation Builder. By placing two markers at the start and end of the transition we measure the difference in QH turn on energy = 77.3 uJ. Similarly, for the QH turn off energy. The conduction power is calculated as P = V_{ON} x I_S. This is integrated to generate Energy. We place markers either side of the on period, and determine the QH conduction energy as 83.9us.

We calculate the QF output capacitance form the voltage resonant frequency:

$\mathbf{C_{QH}} = \frac{1}{(2\pi f)^2\,\mathbf{L_{bl}}}$ We have already measure L_{bl}. We find C_{QH} = 950 pF.



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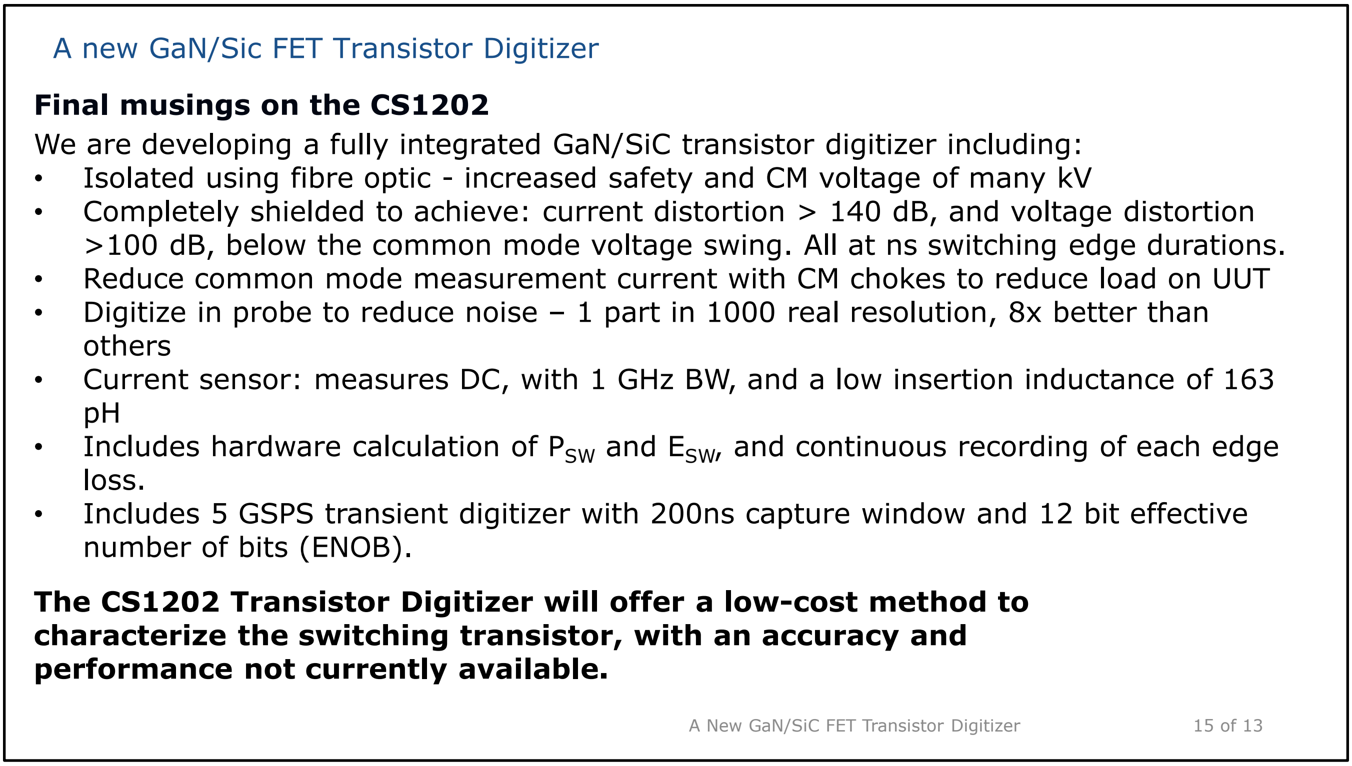
After all this wondering and working out, the CS1202 Transistor digitizer

Key Parameters:

- Doesn’t cost too much!
- Doesn’t use too much power
- Can fully characterize transistor operation in a double pulse test (DPT)
- Can continuously measure Peak Is and Vds, loss and R_{DSON}.
- Bandwidth of nearly 1GHz and 5GSPS when it matters.
- Insertion inductance of 160pH
- Noise free resolution of 1 part in 1000

The CS1202 has 4 length optimized probe cables. The V_{DS} and V_{SAT} input signals are joined together at the probe tip for a single connection. We use the CS1501 current sensors for the current channel. We have used a MMCX connected V_{GS} measurement.



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Final musings on the CS1202

We are developing a fully integrated GaN/SiC transistor digitizer including:

- Isolated using fibre optic - increased safety and CM voltage of many kV
- Completely shielded to achieve: current distortion > 140 dB, and voltage distortion >100 dB, below the common mode voltage swing. All at ns switching edge durations.
- Reduce common mode measurement current with CM chokes to reduce load on UUT
- Digitize in probe to reduce noise – 1 part in 1000 real resolution, 8x better than others
- Current sensor: measures DC, with 1 GHz BW, and a low insertion inductance of 163 pH
- Includes hardware calculation of P_{SW} and E_{SW}, and continuous recording of each edge loss.
- Includes 5 GSPS transient digitizer with 200ns capture window and 12 bit effective number of bits (ENOB).

The CS1202 Transistor Digitizer will offer a low-cost method to characterize the switching transistor, with an accuracy and performance not currently available.

All of these parameters have come about as a result of experience (some of it harsh!) in building the earlier single function probes. We think they work!

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This presentation is available at cleverscope.com

Thank you for the attention!

Visit us at booth 7-600.

I‘m pleased to answer your questions:
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Come and see us in Hall 7, Booth 600 to find out what more we are doing!